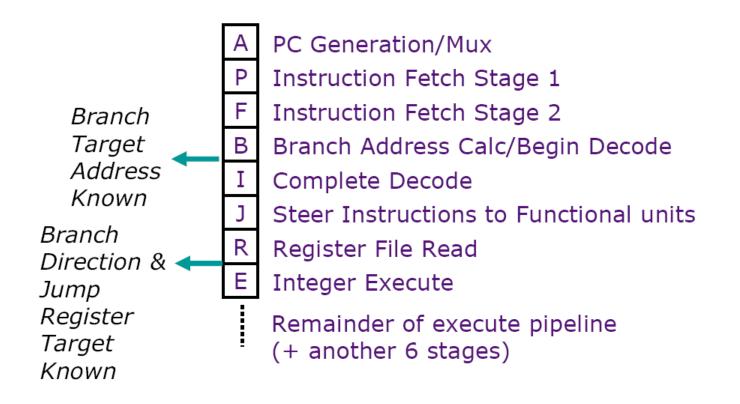
Selected Problems: Branch Prediction, OoO Processing

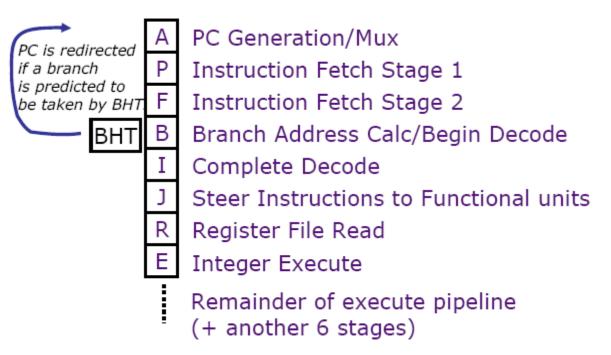
Suvinay Subramanian (adapted from prior 6.823 offerings)

Problem 3.4: Branch Prediction

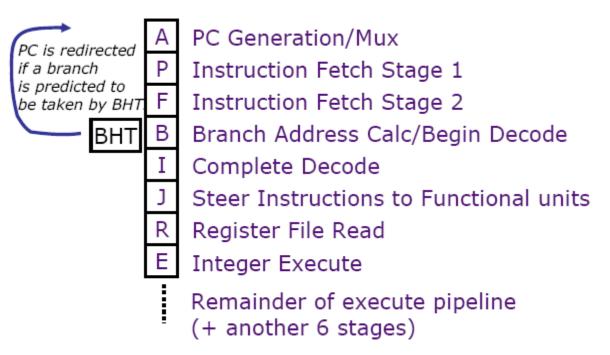
Branch Prediction



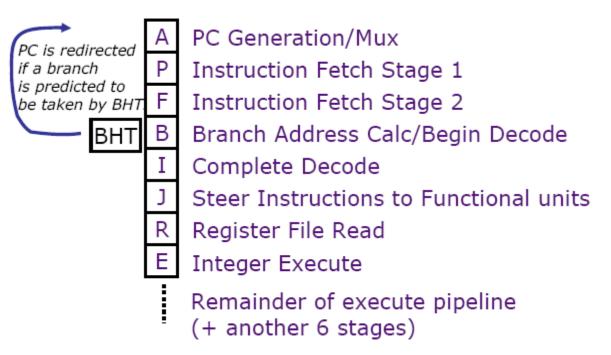
Instruction	Taken known? (At the end of)	Target known? (At the end of)
BEQZ/BNEZ	R	В
J	B (always taken)	В
JR	B (always taken)	R



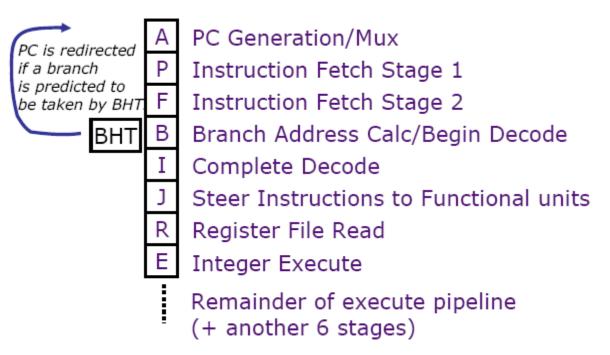
	Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	
BEQZ/	Y	Ν	
BNEZ	N	Y	
	N	Ν	
J	Always taken (No lookup)	Y	
JR	Always taken (No lookup)	Y	



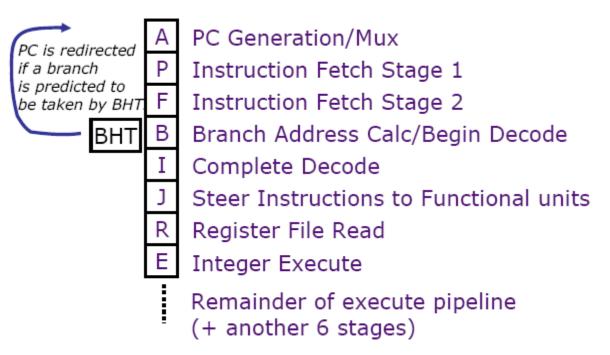
	Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	3
BEQZ/	Y	Ν	
BNEZ	Ν	Y	
	N	Ν	
J	Always taken (No lookup)	Y	
JR	Always taken (No lookup)	Y	



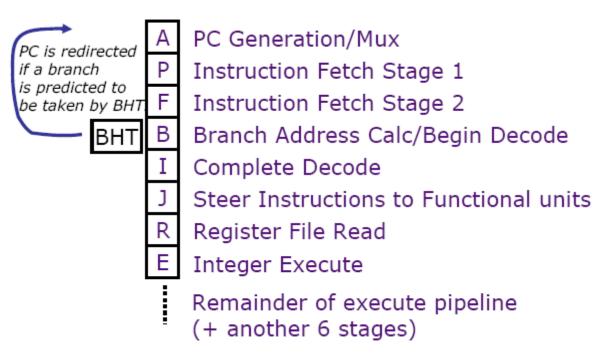
	Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	3
BEQZ/	Y	Ν	6
BNEZ	Ν	Y	
	Ν	Ν	
J	Always taken (No lookup)	Y	
JR	Always taken (No lookup)	Y	



	Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	3
BEQZ/	Y	Ν	6
BNEZ	Ν	Y	6
	Ν	Ν	
J	Always taken (No lookup)	Y	
JR	Always taken (No lookup)	Y	

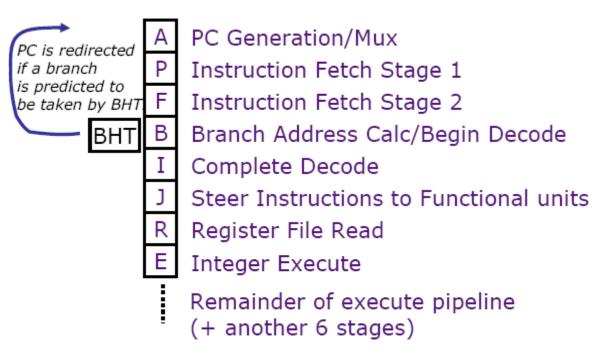


	Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	3
BEQZ/	Y	Ν	6
BNEZ	Ν	Y	6
	Ν	Ν	0
J	Always taken (No lookup)	Y	
JR	Always taken (No lookup)	Y	

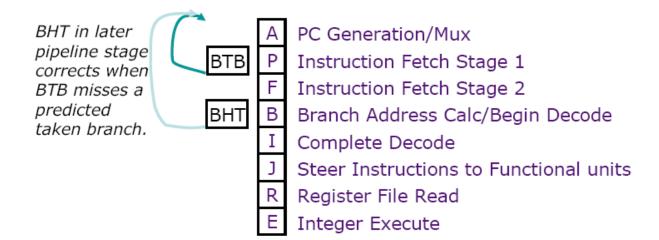


	Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	3
BEQZ/	Y	Ν	6
BNEZ	Ν	Y	6
	Ν	Ν	0
J	Always taken (No lookup)	Y	3
JR	Always taken (No lookup)	Y	

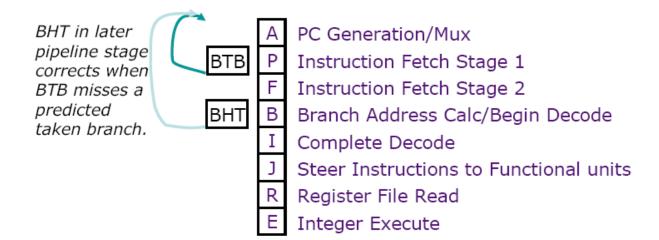
03/18/2016



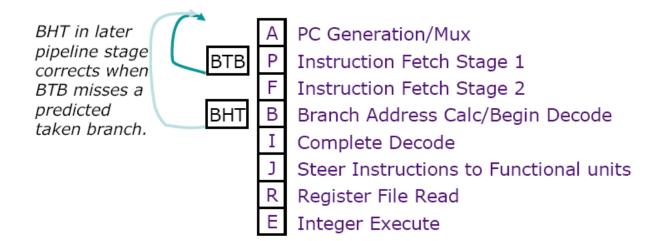
	Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	3
BEQZ/	Y	Ν	6
BNEZ	Ν	Y	6
	Ν	Ν	0
J	Always taken (No lookup)	Y	3
JR	Always taken (No lookup)	Y	6



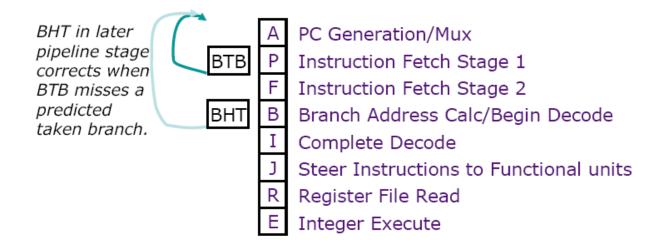
	BTB Hit?	(BHT) Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	Y	
	Y	Y	Ν	
Conditional	Y	N	Y	Cannot occur
Branches	Y	Ν	Ν	Cannot occur
	Ν	Y	Y	
	Ν	Y	Ν	
	Ν	Ν	Y	
	N	N	N	



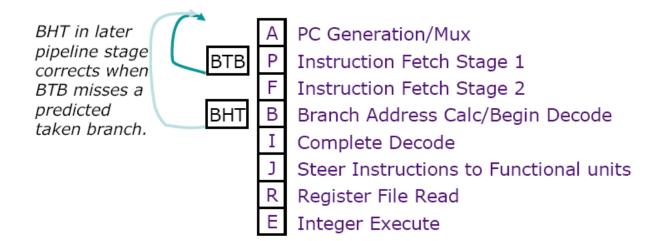
	BTB Hit?	(BHT) Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	Y	1
	Y	Y	Ν	
Conditional	Y	Ν	Y	Cannot occur
Branches	Y	Ν	Ν	Cannot occur
	Ν	Y	Y	
	Ν	Y	Ν	
	Ν	Ν	Y	
	N	Ν	Ν	



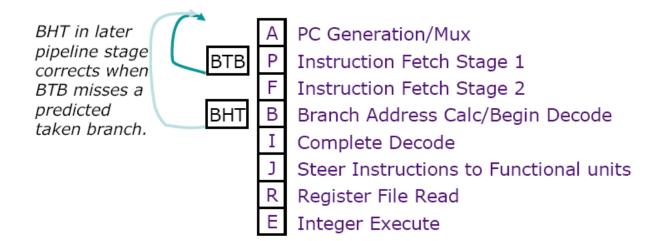
	BTB Hit?	(BHT) Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	Y	1
	Y	Y	Ν	6
Conditional	Y	Ν	Y	Cannot occur
Branches	Y	Ν	Ν	Cannot occur
	Ν	Y	Y	
	Ν	Y	Ν	
	Ν	Ν	Y	
	N	Ν	Ν	



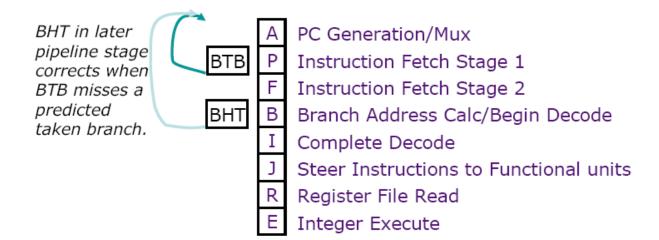
	BTB Hit?	(BHT) Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	Y	1
	Y	Y	Ν	6
Conditional	Y	Ν	Y	Cannot occur
Branches	Y	Ν	Ν	Cannot occur
	Ν	Y	Y	3
	Ν	Y	Ν	
	Ν	Ν	Y	
	Ν	Ν	Ν	



	BTB Hit?	(BHT) Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	Y	1
	Y	Y	Ν	6
Conditional	Y	Ν	Y	Cannot occur
Branches	Y	Ν	Ν	Cannot occur
	Ν	Y	Y	3
	Ν	Y	Ν	6
	Ν	Ν	Y	
	N	N	Ν	

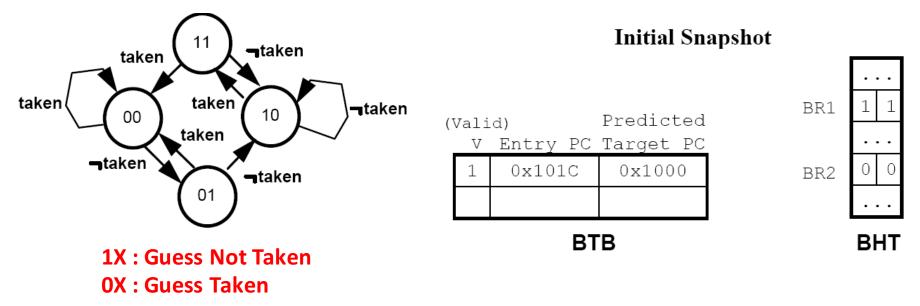


	BTB Hit?	(BHT) Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	Y	1
	Y	Y	Ν	6
Conditional	Y	Ν	Y	Cannot occur
Branches	Y	Ν	Ν	Cannot occur
	Ν	Y	Y	3
	Ν	Y	Ν	6
	Ν	Ν	Y	6
	Ν	Ν	Ν	



	BTB Hit?	(BHT) Predicted Taken?	Actually Taken?	Pipeline bubbles
	Y	Y	Y	1
	Y	Y	Ν	6
Conditional	Y	Ν	Y	Cannot occur
Branches	Y	Ν	Ν	Cannot occur
	Ν	Y	Y	3
	Ν	Y	Ν	6
	Ν	Ν	Y	6
	Ν	Ν	Ν	0

ADDRESS		INSTRUCT	ION			
0x1000	BR1:	BEQZ R5,	NEXT	;	always	taken
0x1004		ADDI R4,	R4, #4			
0x1008		MULT R3,	R5, R3			
0x100C		ST R3,	0(R4)			
0x1010		SUBI R5,	R5, #1			
0x1014	NEXT:	ADDI R1,	R1, #1			
0x1018		SLTI R2,	R1, 100	;	repeat	100 times
0x101C	BR2:	BNEZ R2,	BR1			
0x1020		NOP				
0x1024		NOP				
0x1028		NOP				



ADDRESS		INSTRUCTIO	N			BR1 1 1
0x1000	BR1:	BEQZ R5, N	EXT	; alw	ays taken	
0x1004		ADDI R4, R	4, #4			BR2 0 0
0x1008		MULT R3, R	.5 , R3			
0x100C		ST R3, 0	(R4)			
0x1010		SUBI R5, R	5, #1			BHT
0x1014	NEXT:	ADDI R1, R	1, #1			
0x1018		SLTI R2, R	1, 100	; rep	eat 100 tir	nes
0x101C	BR2:	BNEZ R2, B	R1			edicted
0x1020		NOP			(Valid) Pr V Entry PC Ta	
0x1024		NOP			1 0x101c ()x1000
0x1028		NOP				
					BTB	

		TIN	ИЕ –	>																				
Address	Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0x1000	BEQZ R5, NEXT	A	Ρ	F	В	Ι	J	R	E															
0x1014	ADDI R1, R1, #1																							
0x1018	SLTI R2, R1, 100																							
0x101C	BNEZ R2, LOOP																							
0x1000	BEQZ R5, NEXT																							
0x1014	ADDI R1, R1, #1																							

ADDRESS		INSTRUCTION			BR1 0 (С
0x1000	BR1:	BEQZ R5, NEX	KT ;	always	taken	
0x1004		ADDI R4, R4,	#4		BR2 0 0	С
0x1008		MULT R3, R5,	R3			
0x100C		ST R3, 0(F	34)			
0x1010		SUBI R5, R5,	#1		BH	Т
0x1014	NEXT:	ADDI R1, R1,	#1			
0x1018		SLTI R2, R1,	100 ;	repeat	100 times	
0x101C	BR2:	BNEZ R2, BR1			Ducchisted	
0x1020		NOP		(Valid) V En	Predicted htry PC Target PC	
0x1024		NOP		1 ()x101c 0x1000	
0x1028		NOP		1 ()x1000 0x1014	
					BTB	

		TIN	ИЕ –	>																				
Address	Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0x1000	BEQZ R5, NEXT	A	Ρ	F	В	Ι	J	R	Ε															
0x1014	ADDI R1, R1, #1																							
0x1018	SLTI R2, R1, 100																							
0x101C	BNEZ R2, LOOP																							
0x1000	BEQZ R5, NEXT																							
0x1014	ADDI R1, R1, #1																							

ADDRESS		INSTRUCTION			BR1 0 0
0x1000	BR1:	BEQZ R5, NEX	T ; al	ways taken	
0x1004		ADDI R4, R4,	#4		BR2 0 0
0x1008		MULT R3, R5,	R3		
0x100C		ST R3, 0(R	4)		
0x1010		SUBI R5, R5,	#1		BHT
0x1014	NEXT:	ADDI R1, R1,	#1		
0x1018		SLTI R2, R1,	100 ; re	peat 100 tin	nes
0x101C	BR2:	BNEZ R2, BR1		Dra	
0x1020		NOP		(Valid) Pro V Entry PC Ta	edicted rget PC
0x1024		NOP			x1000
0x1028		NOP		1 0x1000 0	x1014
				BTB	

		TIN	ИЕ –	>																				
Address	Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0x1000	BEQZ R5, NEXT	A	Ρ	F	В	Ι	J	R	Ε															
0x1014	ADDI R1, R1, #1								Α	Ρ	F	В	I	J	R	Ε								
0x1018	SLTI R2, R1, 100																							
0x101C	BNEZ R2, LOOP																							
0x1000	BEQZ R5, NEXT																							
0x1014	ADDI R1, R1, #1																							

					ВТВ	
0x1028		NOP			1 0x1000	0x1014
0x1024		NOP			1 0x101c	0x1000
0x1020		NOP			(Valid) Pr V Entry PC Ta	
0x101C	BR2:	BNEZ R2,	BR1			redicted
0x1018		SLTI R2,	R1, 100	; rep	peat 100 tin	mes
0x1014	NEXT:	ADDI R1,	R1, #1			
0x1010		SUBI R5,	R5, #1			BHT
0x100C		ST R3,	0(R4)			
0x1008		MULT R3,	R5, R3			
0x1004		ADDI R4,	R4, #4			BR2 0 0
0x1000	BR1:	BEQZ R5,	NEXT	; alv	ways taken	
ADDRESS		INSTRUCT	ION			BR1 0 0

		TIN	ИЕ –	>																				
Address	Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0x1000	BEQZ R5, NEXT	A	Ρ	F	В	Ι	J	R	Ε															
0x1014	ADDI R1, R1, #1								Α	Ρ	F	В	I	J	R	Ε								
0x1018	SLTI R2, R1, 100									Α	Ρ	F	В	T	J	R	Ε							
0x101C	BNEZ R2, LOOP																							
0x1000	BEQZ R5, NEXT																							
0x1014	ADDI R1, R1, #1]																	

					BTB	
0x1028		NOP			1 0x1000 (0x1014
0x1024		NOP			1 0x101c (0x1000
0x1020		NOP			(Valid) Pr V Entry PC Ta	
0x101C	BR2:	BNEZ R2, E	BR1			edicted
0x1018		SLTI R2, R	R1, 100	; rep	beat 100 tim	nes
0x1014	NEXT:	ADDI R1, F	R1, #1			
0x1010		SUBI R5, R	₹5 , #1			BHT
0x100C		ST R3, 0	(R4)			
0x1008		MULT R3, F	₹5 , R3			
0x1004		ADDI R4, F	R4, #4			BR2 0 0
0x1000	BR1:	BEQZ R5, N	JEXT	; alw	ways taken	
ADDRESS		INSTRUCTIO	DN			BR1 0 0

		TIN	ИЕ –	>																				
Address	Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0x1000	BEQZ R5, NEXT	A	Ρ	F	В	Ι	J	R	Ε															
0x1014	ADDI R1, R1, #1								Α	Ρ	F	В	I	J	R	Ε								
0x1018	SLTI R2, R1, 100									Α	Ρ	F	В	I	J	R	Ε							
0x101C	BNEZ R2, LOOP										Α	Ρ	F	В	I	J	R	Ε						
0x1000	BEQZ R5, NEXT																							
0x1014	ADDI R1, R1, #1																							

					BTB	
0x1028		NOP			1 0x1000 (0x1014
0x1024		NOP			1 0x101c (0x1000
0x1020		NOP			(Valid) Pr V Entry PC Ta	
0x101C	BR2:	BNEZ R2, E	BR1			edicted
0x1018		SLTI R2, R	R1, 100	; rep	beat 100 tim	nes
0x1014	NEXT:	ADDI R1, F	R1, #1			
0x1010		SUBI R5, R	₹5 , #1			BHT
0x100C		ST R3, 0	(R4)			
0x1008		MULT R3, F	₹5 , R3			
0x1004		ADDI R4, F	R4, #4			BR2 0 0
0x1000	BR1:	BEQZ R5, N	JEXT	; alw	ways taken	
ADDRESS		INSTRUCTIO	DN			BR1 0 0

		TIN	ИЕ –	>																				
Address	Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0x1000	BEQZ R5, NEXT	A	Ρ	F	В	Ι	J	R	E															
0x1014	ADDI R1, R1, #1								Α	Ρ	F	В	I	J	R	Ε								
0x1018	SLTI R2, R1, 100									Α	Ρ	F	В	I	J	R	Ε							
0x101C	BNEZ R2, LOOP										Α	Ρ	F	В	I	J	R	Ε						
0x1000	BEQZ R5, NEXT																							
0x1014	ADDI R1, R1, #1																							

ADDRESS		INSTRUCTION			BR1 0 0
0x1000	BR1:	BEQZ R5, NEXT	; alv	ways taken	
0x1004		ADDI R4, R4, #4			BR2 0 0
0x1008		MULT R3, R5, R3			
0x100C		ST R3, 0(R4)			
0x1010		SUBI R5, R5, #1			BHT
0x1014	NEXT:	ADDI R1, R1, #1			
0x1018		SLTI R2, R1, 10	0 ; rep	peat 100 tim	nes
0x101C	BR2:	BNEZ R2, BR1		De	
0x1020		NOP		(Valid) Provide Alignment (Valid) Provide Al	edicted rget PC
0x1024		NOP		1 0x101c 0)x1000
0x1028		NOP		1 0x1000 C)x1014
				ВТВ	
				1	

		TIN	ИЕ –	>																				
Address	Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0x1000	BEQZ R5, NEXT	A	Ρ	F	В	Ι	J	R	E															
0x1014	ADDI R1, R1, #1								Α	Ρ	F	В	I	J	R	Ε								
0x1018	SLTI R2, R1, 100									Α	Ρ	F	В	I	J	R	Ε							
0x101C	BNEZ R2, LOOP										Α	Ρ	F	В	I	J	R	Ε						
0x1000	BEQZ R5, NEXT												Α	Ρ	F	В	I	J	R	Ε				
0x1014	ADDI R1, R1, #1																							

ADDRESS		INSTRUCTION			BR1 0 0
0x1000	BR1:	BEQZ R5, NEXT	; al	ways taken	
0x1004		ADDI R4, R4, #4			BR2 0 0
0x1008		MULT R3, R5, R3			
0x100C		ST R3, 0(R4)			
0x1010		SUBI R5, R5, #1			BHT
0x1014	NEXT:	ADDI R1, R1, #1			
0x1018		SLTI R2, R1, 10	0 ; rej	peat 100 tin	nes
0x101C	BR2:	BNEZ R2, BR1		De	
0x1020		NOP		(Valid) Pro V Entry PC Ta	edicted rget PC
0x1024		NOP		1 0x101c 0	x1000
0x1028		NOP		1 0x1000 0	x1014
				ВТВ	
				1	

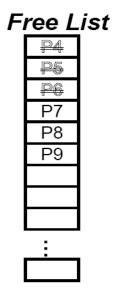
		TIN	ИЕ –	>																				
Address	Instruction	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0x1000	BEQZ R5, NEXT	A	P	F	В	Ι	J	R	E															
0x1014	ADDI R1, R1, #1								Α	Ρ	F	В	I	J	R	Ε								
0x1018	SLTI R2, R1, 100									Α	Ρ	F	В	I	J	R	Ε							
0x101C	BNEZ R2, LOOP										Α	Ρ	F	В	I	J	R	Ε						
0x1000	BEQZ R5, NEXT												Α	Ρ	F	В	I	J	R	Ε				
0x1014	ADDI R1, R1, #1														Α	Ρ	F	В	I	J	R	Ε		

Problem 3.6: Out-of-order execution with Physical register file

Re	enar	тe	Table
R1	P1	P4	
R2	<u>P2</u>	P5	
R3	P3	P6	
R4	P0		

loop:]w	r1, 0 (r2)
	addi begz	r2, r2, 4 r1, skip
	addi	r3, r3, 1
skip:	bne	r2, r4, loop

Ph	nysical Reg	S
P0	8016	р
P1	6823	р
P2	8000	р
P3	7	р
P4		
P5		
P6		
P7		
P8		
P9		



Reorder Buffer (ROB)

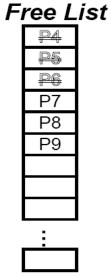
				,0,40	Du		· · · ·	·/			
		use	ex	ор	р1	PR1	p2	PR2	Rd	LPRd	PRd
next to	\rightarrow	Х		lw	р	P2			r1	P1	P4
commit		Х		addi	р	P2			r2	P2	P5
	-	Х		beqz		P4					
		Х		addi	р	P3			r3	P3	P6
next		Х		bne		P5	р	P0			
available	\rightarrow										
	-										
	6	5 873 Sr	ring 2	016	-						28

1. The first three instructions from the next loop iteration are issued into the ROB.

Re	Rename Table						
R1	P1	P4					
R2	<u>P2</u>	P5					
R3	P3	P6					
R4	P0						

loop:	٦w	r1, 0 (r2)
	addi	r2, r2, 4
	beqz	r1, skip
	addi	r3, r3, 1
skip:	bne	r2, r4, loop

Ph	nysical Reg	S
P0	8016	р
P1	6823	р
P2	8000	р
P3	7	р
P4		
P5		
P6		
P7		
P8		
P9		



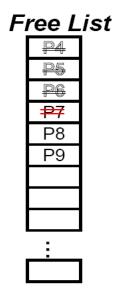
Reorder Buffer (ROB)											
		use	ex	ор	р1	PR1	p2	PR2	Rd	LPRd	PRd
next to	\rightarrow	Х		lw	р	P2			r1	P1	P4
commit		Х		addi	р	P2			r2	P2	P5
		Х		beqz		P4					
		Х		addi	р	P3			r3	P3	P6
next		Х		bne		P5	р	P0			
available	\rightarrow										

1. The first three instructions from the next loop iteration are issued into the ROB.

Re	Rename Table						
R1	P1	₽4	P7				
R2	<u>P2</u>	P5					
R3	<u>P</u> 3	P6					
R4	P0						

loop:	٦w	r1, 0 (r2)
	addi	r2, r2,	4
	beqz	r1, ski	р
	addi	r3, r3,	1
skip:	bne	r2, r4,	Тоор

nysical Reg	S
8016	р
6823	р
8000	р
7	р
	6823



Reorder Buffer (ROB) use ex op p1 PR1 p2 PR2 Rd LPRd PRd

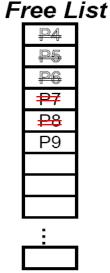
next to	\rightarrow	Х		lw	р	P2			r1	P1	P4
commit		Х		addi	р	P2			r2	P2	P5
		Х		beqz		P4					
		Х		addi	р	P3			r3	P3	P6
next		Х		bne		P5	р	P0			
available	\rightarrow	X		lw		P5			r1	P4	P7
	- A										
		. 012 Cr	wing (0016							20

1. The first three instructions from the next loop iteration are issued into the ROB.

Rename Table						
R1	P1	₽4	P7			
R2	<u>P2</u>	₽5	P8			
R3	P3	P6				
R4	P0					

loop:	٦w	r1, 0 (r2)
	addi	r2, r2, 4
	beqz	r1, skip
	addi	r3, r3, 1
skip:	bne	r2, r4, loop

Ph	nysical Reg	S
P0	8016	р
P1	6823	р
P2	8000	р
P3	7	р
P4		
P5		
P6		
P7		
P8		
P9		



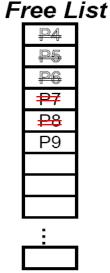
Reorder Buffer (ROB) p1 PR1 p2 PR2 Rd LPRd PRd use ex op next to lw P2 P1 P4 r1 р Х commit P2 r2 P2 addi P5 Х р P4 beqz Х P3 r3 P3 addi P6 р Х P5 P0 next bne Х р available **P5 P7** r1 **P4** Х lw **P5** r2 **P5 P8** Х addi

1. The first three instructions from the next loop iteration are issued into the ROB.

Rename Table						
R1	P1	₽4	P7			
R2	<u>P2</u>	₽5	P8			
R3	P3	P6				
R4	P0					

loop:	٦w	r1, 0 (r2)
	addi	r2, r2, 4
	beqz	r1, skip
	addi	r3, r3, 1
skip:	bne	r2, r4, loop

Ph	Physical Regs					
P0	8016	р				
P1	6823	р				
P2	8000	р				
P3	7	р				
P4						
P5						
P6						
P7						
P8						
P9						



Reorder Buffer (ROB) p1 PR1 p2 PR2 Rd LPRd use ex op next to lw P2 P1 r1 р Х commit P2 r2 P2 addi Х р P4 beqz Х P3 r3 P3 addi р Х P5 P0 next bne Х р available **P5** r1 **P4** Х lw **P5** r2 **P5** Х addi beqz **P7**

Х

PRd

P4

P5

P6

P7

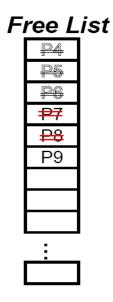
P8

2. All instructions which are ready execute.

Rename Table							
R1	P1	₽4	P7				
R2	<u>P2</u>	₽5	P8				
R3	P3	P6					
R4	P0						

loop:	٦w	r1, 0 (r2)
	addi	r2, r2, 4
	beqz	r1, skip
	addi	r3, r3, 1
skip:	bne	r2, r4, loop

Ph	Physical Regs					
P0	8016	р				
P1	6823	р				
P2	8000	р				
P3	7	р				
P4						
P5						
P6						
Ρ7						
P8						
P9						



Reorder Buffer (ROB)

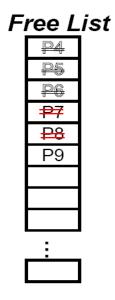
					_			· /			
	_	use	ex	ор	р1	PR1	p2	PR2	Rd	LPRd	PRd
next to	\rightarrow	Х		lw	р	P2			r1	P1	P4
commit		Х		addi	р	P2			r2	P2	P5
	-	Х		beqz		P4					
		Х		addi	р	P3			r3	P3	P6
next		Х		bne		P5	р	P0			
available	\mapsto	Х		lw		P5			r1	P4	P7
		Х		addi		P5			r2	P5	P 8
	\setminus	Х		beqz		P7					
	À										
6 823 Spring 2016 33						33					

2. All instructions which are ready execute.

Rename Table							
R1	P1	₽4	P7				
R2	<u>P2</u>	₽5	P8				
R3	P3	P6					
R4	P0						

loop:	٦w	r1, 0 (r2)	
	addi	r2, r2, 4	
	beqz	r1, skip	
	addi	r3, r3, 1	
skip:	bne	r2, r4, loop	

Ph	Physical Regs					
P0	8016	р				
P1	6823	р				
P2	8000	р				
P3	7	р				
P4						
P5						
P6						
Ρ7						
P8						
P9						



Reorder Buffer (ROB)

				,01 401	Du		(UL	'			
	_	use	ex	ор	р1	PR1	p2	PR2	Rd	LPRd	PRd
next to	\rightarrow	Х	X	lw	р	P2			r1	P1	P4
commit		Х	X	addi	р	P2			r2	P2	P5
	-	Х		beqz		P4					
		Х	X	addi	р	P3			r3	P3	P6
next		Х		bne		P5	р	P0			
available	\rightarrow	X		lw		P5			r1	P4	P7
	$\left \right\rangle$	X		addi		P5			r2	P5	P 8
	\setminus	Х		beqz		P7					
	1										
6.823 Spring 2016 34							34				

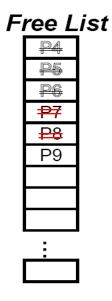
6.823 Spring 2010

2. All instructions which are ready execute.

Rename Table							
R1	P1	₽4	P7				
R2	<u>P2</u>	₽5	P8				
R3	P3	P6					
R4	P0						

loop:	٦w	r1, 0 (r2)
	addi	r2, r2, 4
	beqz	r1, skip
	addi	r3, r3, 1
skip:	bne	r2, r4, loop

Ph	Physical Regs						
P0	8016	р					
P1	6823	р					
P2	8000	р					
P3	7	р					
P4	0	р					
P5	8004	р					
P6	8	р					
P7							
P8							
P9							



Reorder Buffer (ROB) se ex op p1 PR1 p2 PR2

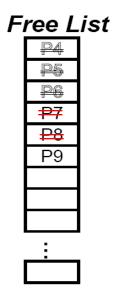
		use	ex	ор	р1	PR1	p2	PR2	Rd	LPRd	PRd
next to	\rightarrow	Х	X	lw	р	P2			r1	P1	P4
commit		Х	X	addi	р	P2			r2	P2	P5
	-	Х		beqz		P4					
		Х	Х	addi	р	P3			r3	P3	P6
next		Х		bne		P5	р	P0			
available	\rightarrow	X		lw		P5			r1	P4	P7
		X		addi		P5			r2	P5	P8
		X		beqz		P7					
	1										
	6	5 873 Sr	ring 2	016							35

2. All instructions which are ready execute.

Rename Table							
R1	P1	₽4	P7				
R2	<u>P2</u>	₽5	P8				
R3	P3	P6					
R4	P0						

loop:	٦w	r1, 0 (r2)
	addi	r2, r2, 4
	beqz	r1, skip
	addi	r3, r3, 1
skip:	bne	r2, r4, loop

Ph	Physical Regs						
P0	8016	р					
P1	6823	р					
P2	8000	р					
P3	7	р					
P4	0	р					
P5	8004	р					
P6	8	р					
P7							
P8							
P9							



Reorder Buffer (ROB)useexopp1PR1p2PR2RdLPRdPRdxXIwpP2r1P1P4

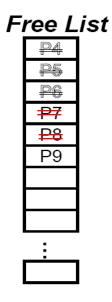
				- 1-	r •		<u> </u>				1 1 1 1 1
next to	\rightarrow	Х	X	lw	р	P2			r1	P1	P4
commit		Х	X	addi	р	P2			r2	P2	P5
	-	Х		beqz	р	P4					
		Х	Х	addi	р	P3			r3	P3	P6
next		Х		bne	р	P5	р	P0			
available	\rightarrow	X		lw	р	P5			r1	P4	P7
	\setminus	X		addi	р	P5			r2	P5	P 8
	\setminus	Х		beqz		P7					
	Ż										
				016							2.6

3. As many instructions as possible commit.

Rename Table							
R1	P1	₽4	P7				
R2	<u>P2</u>	₽5	P8				
R3	P3	P6					
R4	P0						

loop:	٦w	r1, 0 (r2)
	addi	r2, r2, 4
	beqz	r1, skip
	addi	r3, r3, 1
skip:	bne	r2, r4, loop

Ph	Physical Regs						
P0	8016	р					
P1	6823	р					
P2	8000	р					
P3	7	р					
P4	0	р					
P5	8004	р					
P6	8	р					
Ρ7							
P8							
P9							



Reorder Buffer (ROB)

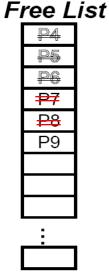
	_	use	ex	ор	р1	PR1	p2	PR2	Rd	LPRd	PRd
next to	\rightarrow	Х	X	lw	р	P2			r1	P1	P4
commit		Х	X	addi	р	P2			r2	P2	P5
	-	Х		beqz	р	P4					
		Х	X	addi	р	P3			r3	P3	P6
next		Х		bne	р	P5	р	P0			
available	\rightarrow	X		lw	р	P5			r1	P4	P7
		Х		addi	р	P5			r2	P5	P8
	\setminus	Χ		beqz		P7					
	1										
6 823 Spring 2016 37							37				

3. As many instructions as possible commit.

Rename Table							
R1	P1	₽4	P7				
R2	<u>P2</u>	₽5	P8				
R3	P3	P6					
R4	P0						

loop:	٦w	r1, 0 (r2)
	addi	r2, r2, 4
	beqz	r1, skip
	addi	r3, r3, 1
skip:	bne	r2, r4, loop

Ph	Physical Regs					
P0	8016	р				
P1	6823	р				
P2	8000	р				
P3	7	р				
P4	0	р				
P5	8004	р				
P6	8	р				
P7						
P8						
P9						



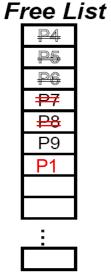
Reorder Buffer (ROB) PR1 p2 PR2 Rd LPRd p1 PRd ор use ex next to lw P2 P1 P4 Χ r1 ≍ р commit P2 r2 P2 P5 Х Х addi р р P4 beqz Х Χ P3 r3 P3 P6 addi Х р P5 P0 next bne Х р р available р **P5 P7** r1 **P4** Х lw р **P5** r2 **P5 P8** Х addi **P7** Х beqz

3. As many instructions as possible commit.

Rename Table						
R1	P1	₽4	P7			
R2	<u>P2</u>	₽5	P8			
R3	P3	P6				
R4	P0					

loop:	٦w	r1, 0 (r2)
	addi	r2, r2, 4
	beqz	r1, skip
	addi	r3, r3, 1
skip:	bne	r2, r4, loop

Ph	Physical Regs					
P0	8016	р				
P1	6823	p				
P2	8000	р				
P3	7	р				
P4	0	р				
P5	8004	р				
P6	8	р				
Ρ7						
P8						
P9						



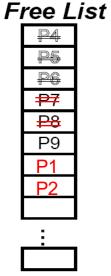
			Re	eorder	Bu	ffer (l	ROE	3)			
	_	use	ex	ор	р1	PR1	p2	PR2	Rd	LPRd	PRd
next to	\rightarrow	*	X	lw	р	P2			r1	P1	P4
commit	Z	Х	X	addi	р	P2			r2	P2	P5
	-	Х		beqz	р	P4					
		Х	Х	addi	р	P3			r3	P3	P6
next		Х		bne	р	P5	р	P0			
available	\rightarrow	X		lw	р	P5			r1	P4	P7
		X		addi	р	P5			r2	P5	P8
	\setminus	X		beqz		P7					
	1										
	-	- 0 <u>-</u> 0 - 0.		010							20

3. As many instructions as possible commit.

Rename Table					
R1	P1	₽4	P7		
R2	<u>P2</u>	₽5	P 8		
R3	P3	P6			
R4	P0				

loop:	٦w	r1, 0 (r2)
	addi	r2, r2, 4
	beqz	r1, skip
	addi	r3, r3, 1
skip:	bne	r2, r4, loop

Ph	nysical Reg	S
P0	8016	р
P1	6823	p
P2	8000	p
P3	7	р
P4	0	р
P5	8004	р
P6	8	р
Ρ7		
P8		
P9		



Reorder Buffer (ROB)											
		use	ex	ор	р1	PR1	p2	PR2	Rd	LPRd	PRd
next to	\rightarrow	≭	X	lw	р	P2			r1	P1	P4
commit	$\left[\right]$	≭	X	addi	р	P2			r2	P2	P5
	- 7	Х		beqz	р	P4					
		Х	X	addi	р	P3			r3	P3	P6
next		Х		bne	р	P5	р	P0			
available	\rightarrow	X		lw	р	P5			r1	P4	P7
		X		addi	р	P5			r2	P5	P8
	\setminus	Х		beqz		P7					
	1										
	6	5.823 Sp	pring 2	2016							40

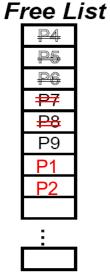
03/18/2016

4. The processor detects that the beqz instruction has been mispredicted, and thus, recovery action is taken.

Rename Table					
R1	P1	₽4	P7		
R2	<u>P2</u>	₽5	P 8		
R3	P3	P6			
R4	P0				

loop:	٦w	r1, 0 (r2)
	addi	r2, r2, 4
	beqz	r1, skip
	addi	r3, r3, 1
skip:	bne	r2, r4, loop

Ph	nysical Reg	S
P0	8016	р
P1	6823	p
P2	8000	p
P3	7	р
P4	0	р
P5	8004	р
P6	8	р
Ρ7		
P8		
P9		



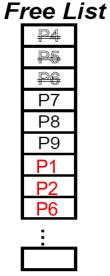
Reorder Buffer (ROB)											
		use	ex	ор	р1	PR1	p2	PR2	Rd	LPRd	PRd
next to	\rightarrow	₩	X	lw	р	P2			r1	P1	P4
commit	$\left[\right]$	*	X	addi	р	P2			r2	P2	P5
	- 7	Х	X	beqz	р	P4					
		Х	Х	addi	р	P3			r3	P3	P6
next		Х		bne	р	P5	р	P0			
available	\mapsto	Х		lw	р	P5			r1	P4	P7
		Х		addi	р	P5			r2	P5	P8
	\setminus	X		beqz		P7					
	1										
		- 022 6		04.6							4.4

4. The processor detects that the beqz instruction has been mispredicted, and thus, recovery action is taken.

Rename Table						
R1	P1	₽4	P4			
R2	<u>P2</u>	₽5	P5			
R3	P3	P6	P3			
R4	P0					

loop:	٦w	r1, 0 (r2)
	addi	r2, r2, 4
	beqz	r1, skip
	addi	r3, r3, 1
skip:	bne	r2, r4, loop

Ph	Physical Regs					
P0	8016	р				
P1	6823	Ρ				
P2	8000	φ				
P3	7	р				
P4	0	р				
P5	8004	р				
P6						
P7						
P8						
P9						



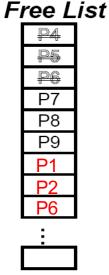
Reorder Buffer (ROB)											
		use	ex	ор	р1	PR1	p2	PR2	Rd	LPRd	PRd
next to	\rightarrow	₩	X	lw	р	P2			r1	P1	P4
commit	\mathbf{X}	*	X	addi	р	P2			r2	P2	P5
	. 7	Х	X	beqz	р	P4					
	1	₩	X	addi	р	P3			r3	P3	P6
next		×		bne	р	P5	р	P0			
available	$ \longrightarrow$	*		lw	р	P5			r1	P4	P7
		*		addi	р	P5			r2	P5	P 8
		₩		beqz		P7					
				04.6							4.0

5. The beqz instruction commits.

Rename Table						
R1	P1	₽4	P4			
R2	<u>P2</u>	₽5	P5			
R3	P3	P6	P3			
R4	P0					

loop:	٦w	r1, 0 (r2)	
	addi	r2, r2, 4	
	beqz	r1, skip	
	addi	r3, r3, 1	
skip:	bne	r2, r4, loop	

Ph	Physical Regs					
P0	8016	р				
P1	6823	Ρ				
P2	8000	φ				
P3	7	р				
P4	0	р				
P5	8004	р				
P6						
P7						
P8						
P9						



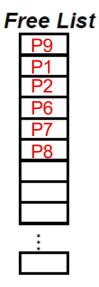
Reorder Buffer (ROB) p1 PR1 p2 PR2 Rd LPRd PRd use ex ор next to lw P2 P1 P4 Χ r1 ≍ р commit P2 r2 P2 P5 Х addi ≍ р beqz р P4 Χ Х Χ P3 r3 P3 P6 addi р × P5 P0 next bne р р × available р **P5 P7** r1 **P4** ≍ lw р **P5** r2 **P5 P8** ≭ addi **P7** ᆂ beqz

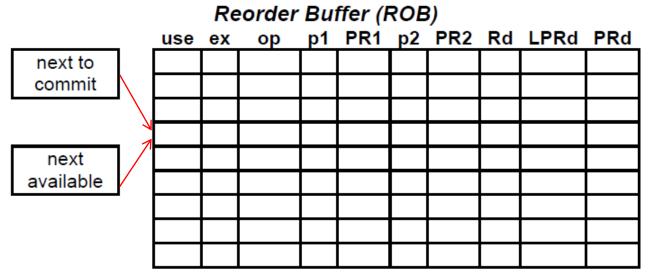
5. The beqz instruction commits.

Rename Table						
R 1	P4					
R2	P5					
R3	P 3					
R4	P0					

loop:	٦w	r1,	0 (r2)
	addi	r2,	r2, 4
	beqz	r1,	skip
	addi	r3,	r3, 1
skip:	bne	r2,	r4, loop

Ph	Physical Regs				
P0	8016	р			
P1					
P2					
P3	7	р			
P4	0	р			
P5	8004	р			
P6					
P7					
P8					
P 9					

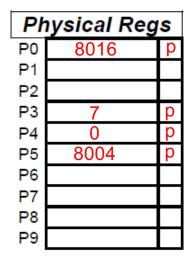


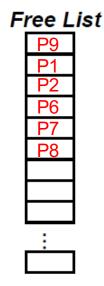


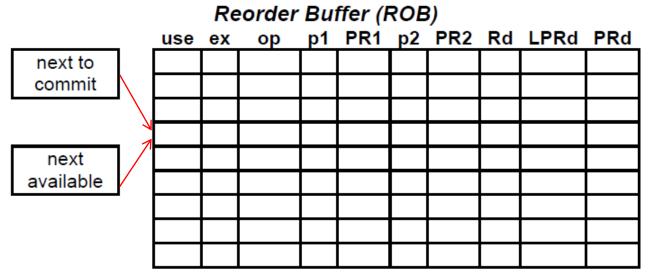
6. The correct next instruction is fetched and is written into the ROB.

Re	Rename Table						
R1	P4						
R2	P5						
R3	P 3						
R4	P0						

loop:	٦w	r1,	0 (r2)
	addi	r2,	r2, 4
	beqz	r1,	skip
	addi	r3,	r3, 1
skip:	bne	r2,	r4, loop



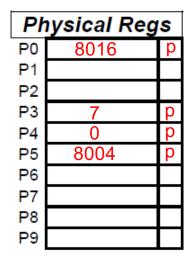


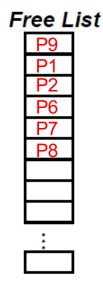


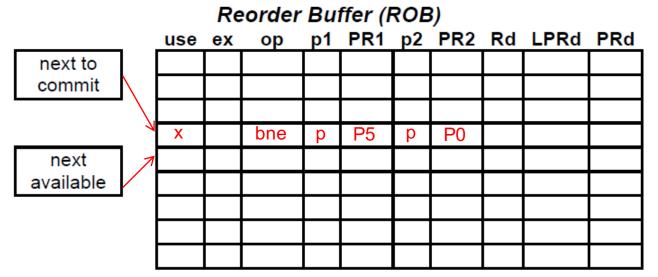
6. The correct next instruction is fetched and is written into the ROB.

Re	Rename Table					
R1	P4					
R2	P5					
R3	P 3					
R4	P0					

loop:	٦w	r1,	0 (r2)
	addi	r2,	r2, 4
	beqz	r1,	skip
	addi	r3,	r3, 1
skip:	bne	r2,	r4, loop







That's all for today...